

WHAT IS CLAIMED IS:

- 1                   1.     An integrated circuit comprising:  
2                   a control block comprising:  
3                         a first series of delay elements coupled to a reference clock input;  
4                         a phase detector coupled to the reference clock input and an output of the  
5 first series of delay elements; and  
6                         a counter coupled to the phase detector and the series of delay elements;  
7                         a storage circuit coupled to the control block and the output of the first series of  
8 delay elements; and  
9                         a delay circuit coupled to the storage circuit.
- 1                   2.     The integrated circuit of claim 1 wherein the storage circuit comprises a  
2 plurality of flip-flops having an input coupled to the counter in the control block, an output  
3 coupled to the delay circuit, and a clock input coupled to an output of the delay circuit.
- 1                   3.     The integrated circuit of claim 1 wherein the storage circuit comprises:  
2                   a logic gate coupled to an input and the output of the delay circuit, and further  
3 coupled to a latch, the latch coupled between the counter in the control circuit and the delay  
4 circuit.
- 1                   4.     The integrated circuit of claim 1 wherein the delay circuit comprises a  
2 series of delay elements, each having an input and an output,  
3                   wherein the storage circuit comprises a logic gate coupled to an input of a delay  
4 element in the delay circuit and an output of a delay element in the delay circuit, and further  
5 coupled to a latch, the latch coupled between the counter in the control circuit and the delay  
6 circuit.
- 1                   5.     The integrated circuit of claim 4 wherein the logic gate is an exclusive-OR  
2 gate.
- 1                   6.     The integrated circuit of claim 1 wherein the delay circuit is a delay  
2 element.

1                    7.        The integrated circuit of claim 6 further comprising:  
2                    a first register having a clock input coupled to an output of the delay circuit; and  
3                    a second register having a complementary clock input coupled the output of the  
4 delay circuit.

1                    8.        The integrated circuit of claim 7 wherein the first register has a first input  
2 and the second register has a second input, and the first and second inputs are coupled to a data  
3 input.

1                    9.        The integrated circuit of claim 8 wherein the integrated circuit is a field  
2 programmable gate array.

1                    10.      An integrated circuit comprising:  
2                    a control circuit configured to receive a reference clock and provide a plurality of  
3 control bits;  
4                    a storage circuit coupled to receive and store the plurality of control bits, and  
5 further configured to provide the plurality of stored control bits; and  
6                    a delay element configured to receive the plurality of stored control bits.

1                    11.      The integrated circuit of claim 10 wherein the control circuit comprises:  
2                    a first series of delay elements configured to receive the reference clock;  
3                    a phase detector configured to compare the phases of the reference clock and an  
4 output of the first series of delay elements and provide an output signal; and  
5                    a counter configured to receive the phase detector output and provide the control  
6 bits.

1                    12.      The integrated circuit of claim 11 wherein a polarity of the phase detector  
2 output depends on the relative phase of the reference clock and the output of the first series of  
3 delay elements, and the counter is an up-down counter that counts up when the phase detector  
4 output has a first polarity, and counts down when the phase detector output has a second polarity.

1                    13.      The integrated circuit of claim 10 wherein the storage circuit comprises a  
2 plurality of flip-flops, each flip-flop having an input configured to receive and store one of the

3 plurality of control bits, and further configured to provide the stored one of the plurality of  
4 control bits to the delay element.

1 14. The integrated circuit of claim 13 wherein each of the plurality of flip-  
2 flops in the storage circuit has a clock input configured to receive the output of the delay  
3 element.

1 15. The integrated circuit of claim 11 further comprising a second series of  
2 delay elements including the delay element, each delay element in the second series of delay  
3 elements having an input, and

4 wherein the storage circuit comprises a logic gate configured to receive a signal  
5 from an input of a delay element in the second series of delay elements and an output of the  
6 second series of delay elements, and further configured to provide an output to a plurality of  
7 latches, each latch configured to receive and store one of the plurality of control bits, and further  
8 configured to provide the stored one of the plurality of control bits to the delay element.

1 16. The integrated circuit of claim 15 wherein the logic gate comprises an  
2 exclusive-OR gate.

1 17. The integrated circuit of claim 10 wherein the control circuit is a delay-  
2 locked loop.

1 18. A method of delaying a data strobe signal comprising:  
2 receiving a reference clock signal;  
3 delaying the reference clock signal a first duration, the first duration dependent on  
4 a plurality of control signals;  
5 comparing the phase the reference clock signal and the delayed reference clock  
6 signal to generate the plurality of control signals;  
7 storing the plurality of control signals;  
8 receiving a data strobe signal; and  
9 delaying the data strobe signal a second duration, the second duration dependent  
10 on the plurality of stored control signals.

1                    19.    The method of claim 18 wherein the plurality of control signals are stored  
2 when the received data strobe signal has been delayed the second duration.

1                    20.    The method of claim 18 wherein the plurality of control signals are stored  
2 when an edge of the data strobe signal is not being delayed.